02-07-00

A

IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

PATENT APPLICATION

Eduard Sackinger

CASE 8

TITLE Active Inductor

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

NEW APPLICATION UNDER 37 CFR § 1.53(b)

Enclosed are the following papers relating to the above-named application for patent:

Specification
[2] Formal Sheets of drawing(s)
[1] Assignment(s) with Cover Sheet
Declaration and Power of Attorney
Information Disclosure Statement

CLAIMS AS FILED				
	NO. FILED	NO. EXTRA	RATE	CALCULATIONS
Total Claims	19 - 20 =	0	x $18 =	$0
Independent Claims	3 - 3 =	0	x $78 =	$0
Multiple Dependent Claims, if applicable			+ $260 =	$0
Basic Fee				$690
			TOTAL FEE	$690

Please file the application and charge **Lucent Technologies Deposit Account No. 12-2325** the amount of $690, to cover the filing fee. Duplicate copies of this letter are enclosed. In the event of non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit **Deposit Account No. 12-2325** as required to correct the error.

The Assistant Commissioner for Patents is hereby authorized to treat any concurrent or future reply, requiring a petition for extension of time under 37 CFR § 1.136 for its timely submission, as incorporating a petition for extension of time for the appropriate length of time if not submitted with the reply.

Please address all correspondence to **Docket Administrator (Room 3C-512), Lucent Technologies Inc., 600 Mountain Avenue, P.O. Box 636, Murray Hill, New Jersey 07974-0636**. However, telephone calls should be made to me at 908-582-4323.

Respectfully,

Eugene J Rosenthal

Eugene J Rosenthal
Reg. No. 36658
Attorney for Applicant(s)

"Express Mail" mailing label number EK552898004US
Date of Deposit 2/4/00
I hereby certify that this Application is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. § 1.10 on the date indicated above and is addressed to the Commissioner of Patents and Trademarks

IRIS F. Thomas
(Typed or printed name of person mailing paper or fee)

Iris F. Thomas
(Signature of person mailing paper or fee)

Date: February 4, 2000
Lucent Technologies Inc.
600 Mountain Avenue (Room 3C-512)
P.O. Box 636
Murray Hill, New Jersey 07974-0636

ACTIVE INDUCTOR

Technical Field

This invention relates to the art of active inductors, and more particularly, to active inductors for use in circuits operating with a low power supply voltage.

Background of the Invention

As is well known, inductors can be used to expand the bandwidth of amplifiers. When an amplifier requiring an inductor is implemented on an integrate circuit, the inductor may be implemented either as spiral inductor or as an active inductor. The problems with using a spiral inductor are that a spiral inductor is large, and its useful frequency range is limited by self resonance. Although active inductors are small, and they typically have a greater frequency range than a spiral inductor, active inductors suffer from the problem of requiring a relatively large voltage drop, with respect to the power supply voltage, across the active inductor. With power supply voltages decreasing, to reduce power consumption, the relatively large voltage drop of prior art active inductors becomes problematic, in that it does not leave enough headroom for the amplifying circuit coupled to the active inductor to operate properly.

Summary of the Invention

I have recognized that an active inductor with a smaller voltage drop with respect to the power supply voltage of an integrated circuit can be realized, in accordance with the principles of the invention, by an active inductor which is biased from a voltage higher than the power supply voltage, the higher voltage being generatable on the integrated circuit. Advantageously, more headroom is left for the amplifying circuit coupled to the active inductor to operate properly than with prior art active inductors. Furthermore, by not simply operating the entire active inductor from a higher voltage, the power dissipation remains the same as if the active inductor were connected as in the prior art only to the power supply voltage, and the task of generating the voltage higher than the power supply voltage is simplified, because only leakage current, e.g., nanoamps, is required.

Brief Description of the Drawing

In the drawing:

FIG. 1 shows an exemplary active inductor arranged in accordance with the principles of the invention so as to realize a smaller voltage drop with respect to the power supply voltage than was achievable by the prior art;

FIG. 2 shows an exemplary active inductor arranged in accordance with the principles of the invention so as to realize a smaller voltage drop with respect to the power supply voltage than was achievable by the prior art that uses the same structure as does FIG. 1 but is modified for use with a PMOS transistor; and

FIG. 3 shows an exemplary embodiment of the high voltage generator of FIG. 1.

Detailed Description

The following merely illustrates the principles of the invention. It will thus be appreciated that those skilled in the art will be able to devise various arrangements which, although not explicitly described or shown herein, embody the principles of the invention and are included within its spirit and scope. Furthermore, all examples and conditional language recited herein are principally intended expressly to be only for pedagogical purposes to aid the reader in understanding the principles of the invention and the concepts contributed by the inventor(s) to furthering the art, and are to be construed as being without limitation to such specifically recited examples and conditions. Moreover, all statements herein reciting principles, aspects, and embodiments of the invention, as well as specific examples thereof, are intended to encompass both structural and functional equivalents thereof. Additionally, it is intended that such equivalents include both currently known equivalents as well as equivalents developed in the future, i.e., any elements developed that perform the same function, regardless of structure.

Thus, for example, it will be appreciated by those skilled in the art that the block diagrams herein represent conceptual views of illustrative circuitry embodying the principles of the invention. Similarly, it will be appreciated that any flow charts, flow diagrams, state transition diagrams, pseudocode, and the like represent various processes which may be substantially represented in computer readable medium and so executed by a computer or processor, whether or not such computer or processor is explicitly shown.

The functions of the various elements shown in the FIGs., including functional blocks labeled as "processors" may be provided through the use of dedicated hardware as well as hardware capable of executing software in association with appropriate software. When provided by a processor, the functions may be provided by a single dedicated processor, by a single shared processor, or by a plurality of individual processors, some

of which may be shared. Moreover, explicit use of the term "processor" or "controller" should not be construed to refer exclusively to hardware capable of executing software, and may implicitly include, without limitation, digital signal processor (DSP) hardware, read-only memory (ROM) for storing software, random access memory (RAM), and non-volatile storage. Other hardware, conventional and/or custom, may also be included. Similarly, any switches shown in the FIGS. are conceptual only. Their function may be carried out through the operation of program logic, through dedicated logic, through the interaction of program control and dedicated logic, or even manually, the particular technique being selectable by the implementor as more specifically understood from the context.

In the claims hereof any element expressed as a means for performing a specified function is intended to encompass any way of performing that function including, for example, a) a combination of circuit elements which performs that function or b) software in any form, including, therefore, firmware, microcode or the like, combined with appropriate circuitry for executing that software to perform the function. The invention as defined by such claims resides in the fact that the functionalities provided by the various recited means are combined and brought together in the manner which the claims call for. Applicant thus regards any means which can provide those functionalities as equivalent as those shown herein.

Unless otherwise explicitly specified herein, the drawings are not drawn to scale.

FIG. 1 shows an exemplary active inductor arranged in accordance with the principles of the invention so as to realize a smaller voltage drop with respect to the power supply voltage than was achievable by the prior art. More specifically, the active inductor is biased from a voltage higher than the power supply voltage, the higher voltage being generatable on the integrated circuit. Shown in FIG. 1 are metal oxide semiconductor (MOS) transistor 101, including gate terminal 103, drain terminal 105, source terminal 107, bulk terminal 109, power supply voltage Vdd, high voltage generator 111, gate resistor 113, and power supply voltage Vss.

Also shown in FIG. 1 is optional amplifying circuit 115, which uses the active inductor as part of its load in performing amplification of input signal 117.

In the embodiment of the invention shown in FIG. 1, MOS transistor 101 is a negative metal oxide semiconductor (NMOS) transistor. Drain terminal 105 is connected to power supply voltage Vdd. An exemplary value for power supply voltage Vdd for use with contemporary integrated circuit technology is, nominally, 2.5V, with Vss being 0V, although other, and in particular, lower power supply voltages are possible. Bulk terminal 109 is coupled to Vss.

High voltage generator 111 is coupled between Vdd and Vss and uses power from the power supply to generate a voltage higher than Vdd. Preferably the higher voltage generated is one threshold voltage above Vdd. Lower "higher voltages" do not give as much headroom, while higher "higher voltages" can cause transistor 101 to stop behaving like an active inductor, e.g., by leaving saturation mode. For example, with a power supply voltage of 2.5V, high voltage generator 111 supplies at its output 3.4V. The generation of the higher voltage by high voltage generator 111 may be performed in any manner desired by the implementor. One such manner is disclosed in FIG. 3 and is described further hereinbelow. Since high voltage generator 111 acts as a voltage source, preferably it has a low output impedance.

Gate resistor 113 is coupled between gate terminal 103 and the output of high voltage generator 111.

In operation, the circuit of FIG. 1 behaves substantially the same as a prior art active inductor which would have the terminal of gate resistor 113 that is not coupled to gate terminal 103 coupled to Vdd. For a detailed description of prior art active inductors see, for example, *Broad-Band Monolithic Microwave Active Indcutor and Its Application to Minaturized Wide-Band Amplifiers* by Hara et al., published in IEEE Tansactions on Microwave Theory and Techniques, Vol. 36, No. 12, pp. 1920-1924, December 1988, which is incorporated by reference as if fully set forth herein. However, because in the circuit of FIG. 1 the terminal of gate resistor 113 that is not coupled to gate terminal 103 is coupled to the higher voltage supplied as an output by high voltage generator 111, the voltage drop between Vdd and source terminal 107 is reduced. Advantageously, this permits greater headroom for the operation of an amplifying circuit, e.g., optional amplifying circuit 115, that uses the active inductor as part of its load.

FIG. 2 shows an exemplary active inductor arranged in accordance with the principles of the invention so as to realize a smaller voltage drop with respect to the power supply voltage than was achievable by the prior art that uses the same structure as does FIG. 1 but is modified for use when MOS transistor 101 is a positive metal oxide semiconductor (PMOS) transistor. Note that elements of FIG. 2 having the same reference numerals as elements of FIG. 1 are the same as described for FIG. 1, execept that MOS transistor 101 is a PMOS transistor in FIG. 2. Given the description of FIG. 1, those of ordinary skill in the art will readily understand and be able to implement active inductors using PMOS transistors as shown in FIG. 2.

FIG. 3 shows an exemplary embodiment of high voltage generator 111. Shown in FIG. 3 are oscillator 301, voltage doubler 303, clamp 305, and ripple filter 307, which are cascaded in sequence in the manner shown. Each of oscillator 301, voltage doubler 303,

clamp 305 and ripple filter 307 are well known in the art, and the particular structure shown within each is for pedagogical purposes only. Coarsely, in idealized operation, the square wave generated by oscillator 301 causes a voltage of twice Vdd to be generated by voltage doubler 303. This voltage is then clamped to one threshold voltage above Vdd by clamp 305, and any ripple from the square wave is filtered out by ripple filter 307. Any particular actual embodiment must, of course, as will be readily recognized by those of ordinary skill in the art, take into account actual circuit operating parameters, especially the voltage drops across the diodes of voltage doubler 303.

What is claimed is:

1. An active inductor for use on an integrated circuit having a power supply voltage supplied from a first power supply terminal, comprising:

an metal oxide semiconductor (MOS) transistor having a gate terminal, a drain terminal, and a source terminal, said drain terminal being coupled to said power supply voltage and said source terminal being one of the terminals of said active inductor; and

a resistor having a first terminal coupled to said gate terminal and a second terminal coupled to a voltage that is derived from said power supply voltage and has a larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage.

2. The invention as defined in claim 1 wherein said other terminal of said active inductor is said first power supply terminal.

3. The invention as defined in claim 1 wherein said MOS transistor also has a bulk terminal, said bulk terminal being connected to a second power supply terminal.

4. The invention as defined in claim 1 wherein MOS transistor is a negative metal oxide semiconductor (NMOS).

5. The invention as defined in claim 1 wherein MOS transistor is a positive metal oxide semiconductor (PMOS).

6. The invention as defined in claim 1 wherein said MOS transistor also has a bulk terminal, said bulk terminal being connected to a second power supply terminal, and wherein said power supply voltage supplied from said first power supply terminal is higher than a voltage supplied from said second power supply terminal.

7. The invention as defined in claim 1 wherein said MOS transistor also has a bulk terminal, said bulk terminal being connected to a second power supply terminal, and wherein said power supply voltage supplied from said first power supply terminal is lower than a voltage supplied from said second power supply terminal.

8. The invention as defined in claim 1 wherein said MOS transistor is a negative metal oxide semiconductor (NMOS), said NMOS transistor also has a bulk terminal, said bulk terminal being connected to a second power supply terminal, and wherein said first power supply terminal is the positive power supply terminal for said integrated circuit and said second power supply terminal is the negative power supply terminal for said integrated circuit.

9. The invention as defined in claim 1 wherein said MOS transistor is a positive metal oxide semiconductor (PMOS), said PMOS transistor also has a bulk terminal, said bulk terminal being connected to a second power supply terminal, and wherein said first power supply terminal is the negative power supply terminal for said integrated circuit and said second power supply terminal is the positive power supply terminal for said integrated circuit.

10. The invention as defined in claim 1 wherein said voltage that is derived from said power supply voltage and has a larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage has a larger absolute value than said power supply by one threshold voltage of said MOS transistor.

11. The invention as defined in claim 1 wherein said voltage that is derived from said power supply voltage is generated from said power supply voltage by a high voltage generator.

12. The invention as defined in claim 1 further including on said integrated circuit a high voltage generator that generates said voltage that has a larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage.

13. The invention as defined in claim 1 further including on said integrated circuit a high voltage generator that generates said voltage that has a larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage, said high voltage generator comprising:

an oscillator generating an oscillating output signal;

a voltage doubler receiving as an input said oscillating output signal from said oscillator and supplying as an output a signal that has an average larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage;

a clamp which receives as an input said output of said voltage doubler and supplies an output voltage substantially clamped to a prescribed value that has a larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage;

and a ripple filter which filters said output of said clamp and supplies the output of said high voltage generator, which said voltage that has a larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage.

14. An active inductor on an integrated circuit, comprising:

a metal oxide semiconductor (MOS) transistor; and

a high voltage generator which generates a voltage outside the range of voltages being supplied to said integrated circuit by a power supply;

wherein said MOS transistor is coupled to said high voltage generator so as to bias said MOS transistor with said voltage outside the range of voltages being supplied to said integrated circuit by a power supply.

15. The invention as defined in claim 14 wherein said high voltage generator comprises:

an oscillator generating an oscillating output signal;

a voltage doubler receiving as an input said oscillating output signal from said oscillator and supplying as an output a voltage signal that has an average voltage that is outside the range of voltages being supplied to said integrated circuit by a power supply;

a clamp which receives as an input said output of said voltage doubler and supplies an output voltage substantially clamped to a prescribed value that is outside the range of voltages being supplied to said integrated circuit by a power supply;

and a ripple filter which filters said output of said clamp and supplies the output of said high voltage generator.

16. An active inductor on an integrated circuit, said active inductor comprising a metal oxide semiconductor (MOS) transistor and being characterized in that said active inductor is biased using a voltage generated on said integrated circuit that is beyond the range of the voltage supplied by a power supply for operating said integrated circuit.

17. The invention as defined in claim 16 wherein said MOS transistor is a negative metal oxide semiconductor (NMOS) transistor

18. The invention as defined in claim 16 wherein said MOS transistor is a positive metal oxide semiconductor (PMOS) transistor

19. The invention as defined in claim 16 wherein said active inductor is biased by coupling a gate of said MOS transistor to said voltage generated on said integrated circuit that is beyond the range of the voltage supplied by a power supply for operating said integrated circuit via an impedance.

Abstract

An active inductor with a smaller voltage drop with respect to the power supply voltage of an integrated circuit can be realized by an active inductor which is biased from a voltage higher than the power supply voltage, the higher voltage being generatable on the integrated circuit. Advantageously, more headroom is left for the amplifying circuit coupled to the active inductor to operate properly than with prior art active inductors. Furthermore, by not simply operating the entire active inductor from a higher voltage, the power dissipation remains the same as if the active inductor were connected as in the prior art only to the power supply voltage, and the task of generating the voltage higher than the power supply voltage is simplified, because only leakage current, e.g., nanoamps, is required.

FIG. 1

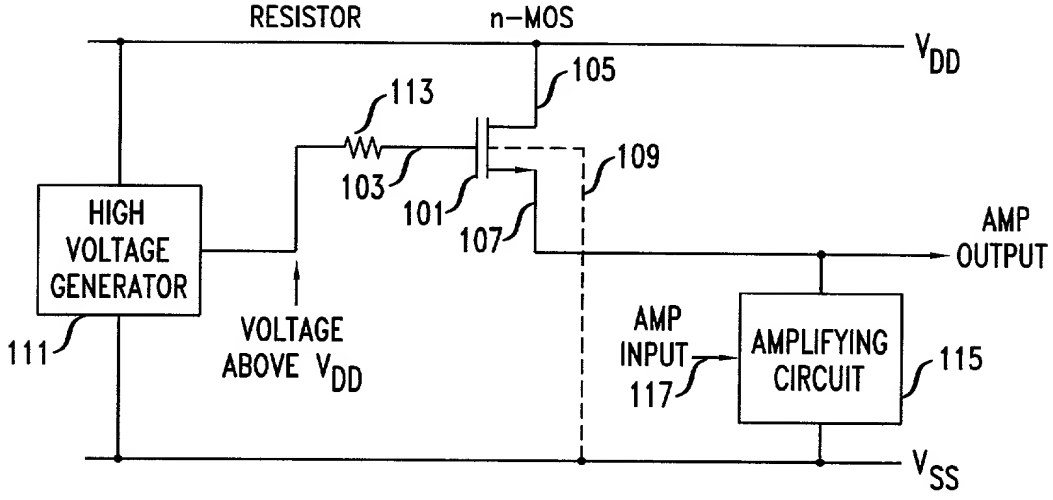
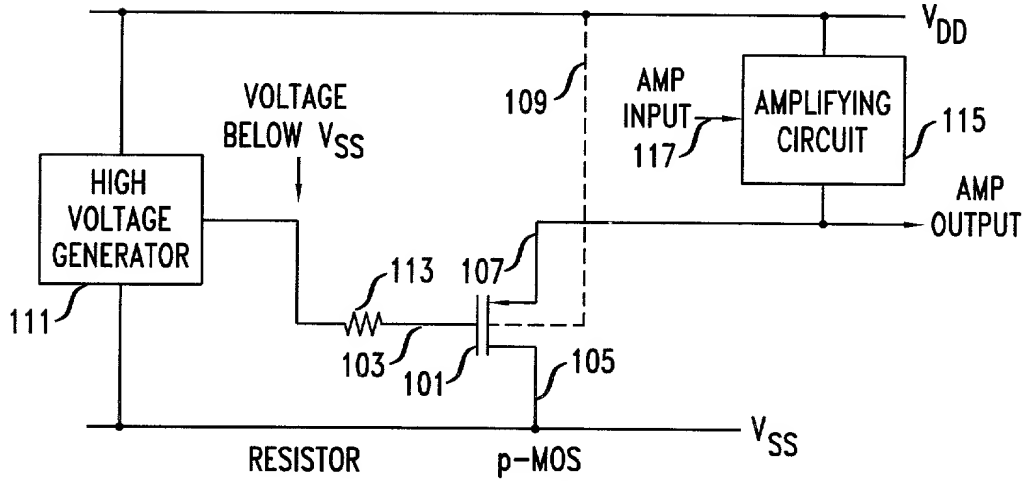

RESISTOR
n-MOS
V_{DD}
105
113
103
101
109
107
HIGH VOLTAGE GENERATOR
AMP OUTPUT
111
VOLTAGE ABOVE V_{DD}
AMP INPUT
117
AMPLIFYING CIRCUIT
115
V_{SS}

FIG. 2


V_{DD}
VOLTAGE BELOW V_{SS}
109
AMP INPUT
117
AMPLIFYING CIRCUIT
115
HIGH VOLTAGE GENERATOR
AMP OUTPUT
113
107
111
103
101
105
V_{SS}
RESISTOR
p-MOS

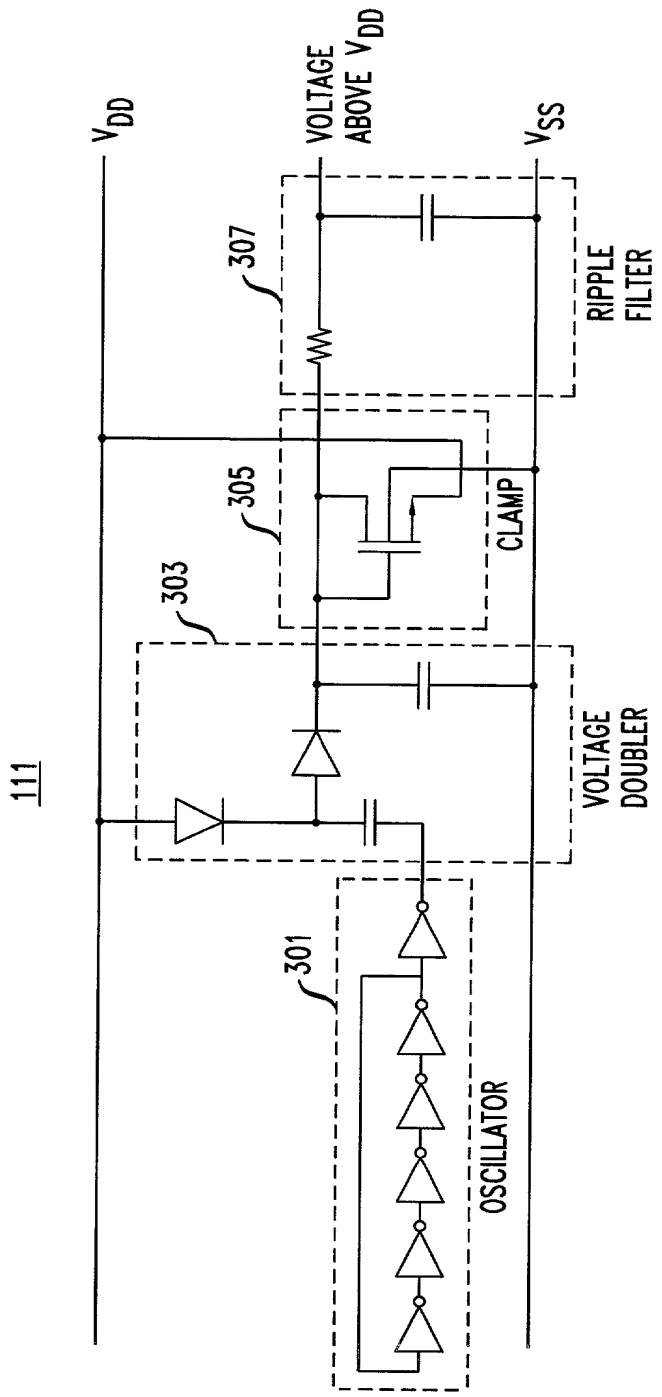

111
V_{DD}
VOLTAGE ABOVE V_{DD}
V_{SS}
307
RIPPLE FILTER
305
CLAMP
303
VOLTAGE DOUBLER
301
OSCILLATOR

FIG. 3

IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

Declaration and Power of Attorney

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am an original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled **Active Inductor** the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by an amendment, if any, specifically referred to in this oath or declaration.

I acknowledge the duty to disclose all information known to me which is material to patentability as defined in Title 37, Code of Federal Regulations, 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

None

I hereby claim the benefit under Title 35, United States Code, 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

None

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint the following attorney(s) with full power of substitution and revocation, to prosecute said application, to make alterations and amendments therein, to receive the patent, and to transact all business in the Patent and Trademark Office connected therewith:

Thomas J. Bean	(Reg. No. 44528)
Lester H. Birnbaum	(Reg. No. 25830)
Richard J. Botos	(Reg. No. 32016)
Jeffery J. Brosemer	(Reg. No. 36096)
Kenneth M. Brown	(Reg. No. 37590)
Craig J. Cox	(Reg. No. 39643)
Donald P. Dinella	(Reg. No. 39961)
Guy H. Eriksen	(Reg. No. 41736)
Martin I. Finston	(Reg. No. 31613)
William S. Francos	(Reg. No. 38456)
Barry H. Freedman	(Reg. No. 26166)
Julio A. Garceran	(Reg. No. 37138)
Jimmy Goo	(Reg. No. 36528)
Anthony Grillo	(Reg. No. 36535)
Stephen M. Gurey	(Reg. No. 27336)
John M. Harman	(Reg. No. 38173)
Matthew J. Hodulik	(Reg. No. 36164)
Michael B. Johannesen	(Reg. No. 35557)
Mark A. Kurisko	(Reg. No. 38944)
Irena Lager	(Reg. No. 39260)
John B. MacIntyre	(Reg. No. 41170)
Christopher N. Malvone	(Reg. No. 34866)
Scott W. McLellan	(Reg. No. 30776)
Martin G. Meder	(Reg. No. 34674)
John C. Moran	(Reg. No. 30782)
Michael A. Morra	(Reg. No. 28975)
Gregory J. Murgia	(Reg. No. 41209)
Claude R. Narcisse	(Reg. No. 38979)
Joseph J. Opalach	(Reg. No. 36229)
Neil R. Ormos	(Reg. No. 35309)
Eugen E. Pacher	(Reg. No. 29964)
Jack R. Penrod	(Reg. No. 31864)
Gregory C. Ranieri	(Reg. No. 29695)
Scott J. Rittman	(Reg. No. 39010)
Ferdinand M. Romano	(Reg. No. 32752)
Eugene J. Rosenthal	(Reg. No. 36658)
Bruce S. Schneider	(Reg. No. 27949)
Ronald D. Slusky	(Reg. No. 26585)
David L. Smith	(Reg. No. 30592)
Ozer M. N. Teitelbaum	(Reg. No. 36698)
John P. Veschi	(Reg. No. 39058)
David Volejnicek	(Reg. No. 29355)
Charles L. Warren	(Reg. No. 27407)
Jeffrey M. Weinick	(Reg. No. 36304)
Eli Weiss	(Reg. No. 17765)

Please address all correspondence to the Docket Administrator (Rm. 3C-512), Lucent Technologies Inc., 600 Mountain Avenue, P. O. Box 636, Murray Hill, New Jersey 07974-0636. Telephone calls should be made to Eugene J Rosenthal by dialing 908-582-4323.

Full name of sole inventor: Eduard Sackinger

Inventor's signature E. Sackinger Date Feb. 3, 2000

Residence: Shrewsbury, Monmouth County, New Jersey

Citizenship: Switzerland

Post Office Address:	326 Crawford Street Shrewsbury, New Jersey, 07724